REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

I. Disposition of Claims

Claims 1, 3-6, 18, 19, and 23-27 are pending in this application. By way of this reply, claims 1, 18, and 19 have been amended.

II. Claim Amendments

Claim 1 has been amended to recite that the "lock detect indicator inputs the system clock." Further, claim 1 has been amended to clarify that the phase-frequency detector inputs a system clock and a chip clock generated by the phase locked loop. No new matter has been added by way of these amendments as support for these amendments may be found, for example, in Figure 3 of the present application.

Claim 18 has been amended to recite that the "detecting means inputs the system clock." No new matter has been added by way of this amendment as support for this amendment may be found, for example, in Figure 3 of the present application.

Claim 19 has been amended to recite that generating a pulse on a lock status signal is "dependent on the system clock." No new matter has been added by way of this amendment as support for this amendment may be found, for example, in paragraph [0035] of the present application.

III. Rejection(s) Under 35 U.S.C § 102

Claims 1, 3, 5, 6, 18, 19, and 23-27 of the present application were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,404,289 issued to Su et al. (hereinafter "Su"). For the reasons set forth below, this rejection is respectfully traversed.

The present invention is generally directed to a technique for determining whether a phase locked loop is in lock or out of lock. With reference to the exemplary embodiment of the present invention shown in Figure 4 of the present application, the flip-flop **112** that generates the lock status signal (indicative of whether the phase locked loop is in lock or out of lock) is clocked by the system clock of the phase locked loop (*see* Figure 3). *See* Specification, paragraph [0035]. Further, the circuitry grouped as stage **80** in Figure 4 of the present application is dependent on the system clock to generate the lock signal, which then serves as an input to the flip-flop **112**. *See* Specification, paragraphs [0028] – [0030], [0035]. Thus, the lock detect indicator of the present invention as shown in Figure 4 of the present application is dependent on the system clock to generate the lock status signal.

Accordingly, amended independent claim 1 of the present application requires that the lock detect indicator input the system clock. Similarly, amended independent claim 18 of the present application requires that the detecting means input the system clock. Further, amended independent claim 19 of the present application requires that generating a pulse on a lock status signal be dependent on the system clock.

Su, in contrast to the present invention, fails to disclose all the limitations of

amended independent claims 1, 18, and 19 of the present application. In Su, the purported lock detect indicator shown in Figure 3 of Su is only dependent on the UP and DOWN signals generated by the phase locked loop phase detector (shown as **220** in Figure 2 of Su). With reference to Figure 3 of Su, Su discusses that OR gate **310**, AND gate **320**, and delay circuit **330** generate a lock detect signal (at the output of AND gate **320**) that indicates an out of lock condition if there is a long pulse on the lock detect signal and a lock condition if there is a short or no pulse on the lock detect signal. *See* Su, column 4, lines 34 – 40. Thus, in Su, the generation of the lock detect signal is not dependent on the system clock serving as an input to the purported lock detect indicator.

Further, with respect to the remaining circuitry of the purported lock detect indicator shown in Figure 3 of Su, one of ordinary skill in the art will note that the flip-flops **340**,**360** used in the purported lock detect indicator are Set-Reset (SR) flip-flops that have no clock input. Instead, SR flip-flops toggle based on signals connected to the Set and Reset inputs. There is no circuitry in the purported lock detect indicator shown in Figure 3 of Su that is dependent on a clock signal. Instead, the purported lock detect indicator of Su operates solely dependent on the pulses on the UP and DOWN signals from the phase locked loop phase detector (shown as **220** in Figure 2 of Su).

However, in the present invention, the generation of the lock status signal is dependent on the system clock as required by amended independent claims 1, 18, and 19 of the present application. This is evident from the fact that the circuitry (*e.g.*, stages **90**, **110**, **120**) of the lock detect indicator shown in Figure 4 of the present application is dependent on the system clock serving as an input to the lock detect indicator.

In view of the above, Su fails to show or suggest the present invention as recited

in amended independent claims 1, 18, and 19 of the present application. Thus, amended independent claims 1, 18, and 19 of the present application are patentable over Su. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Rejection(s) Under 35 U.S.C § 103

Claim 4 of the present application was rejected under 35 U.S.C. § 103(a) as being unpatentable over Su. As discussed above, amended independent claim 1 of the present application patentable over Su. Accordingly, claim 4 of the present application, which depends from amended independent claim 1 of the present application, is allowable for at least the same reasons.

V. Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.139001;P6826).

Respectfully submitted,

Date: 1/16/04

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